Detector Support Group

Weekly Report, 2019-08-21

Summary

Hall A – Super BigBite Spectrometer (SBS) HCAL

- Cut and terminated 80 BNC to LEMO cables.

Hall B – Magnets

- To solve issues with the duplicate/missed timestamps for the data transfer from the FastDAQ cRIO to EPICS the LabVIEW code has been modified.
  - ✶ Updated the library used to read FPGA.
    - ▪ Library allows the ability to output the data as an interleaved 1D array, which should be faster than the 2D array running in the previous version.
  - ✶ In the cRIO EPICS I/O Server, changed data types from Doubles/Arrays of Doubles to Singles/Array of Singles.
  - ✶ Separated FPGA read and send to EPICS to run in two different loops.
  - ✶ With all modifications deployed new LabVIEW program in Torus FastDAQ cRIO and ran test.
    - ▪ Found no duplicate/missed timestamps.
    - ▪ Test will continue for a long run period to ensure that changes in LabVIEW code solved the issues.
- Updated Torus FastDAQ cRIO to Real-Time 2019.
  - ✶ Installed NI software to upgrade Operating System NI Linux Real-Time in the cRIO.

Hall B – Gas Control Systems

- Updated gas control LabVIEW program from version 2018 to version 2019. Code has not been deployed, waiting until the end of the current physics run.

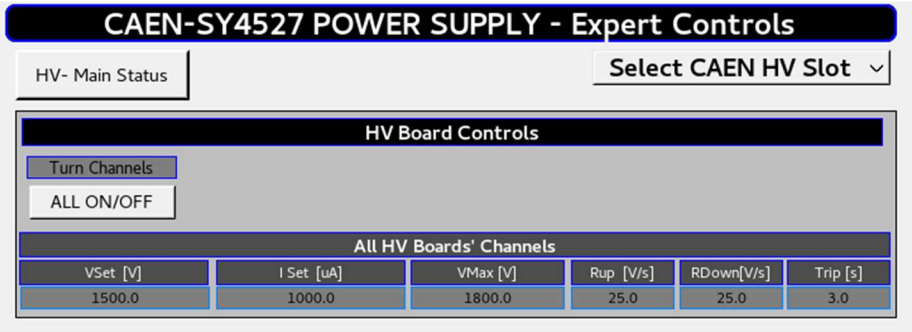
Hall C – CAEN HV Test Station

- Submitted requisition for the load box resistors, HV multiplexer components, and adapters (Radiall 52 pin connector to SHV connector).

Hall C – CAEN HV EPICS Test Station

- Wrote six Java scripts used to set “Vset”, “Imon”,”Vmax”, “RUp”, “RDWn”, and “Trip” parameters for 16 boards’ channels simultaneously.
  - ✶ Above mentioned parameters are set simultaneously for 576 channels during test.
  - ✶ Java scripts run as part of the CSS-BOY screens, when user introduces a value for each parameter.
- Modified two Java scripts to turn on/off all 16 HV boards’ channels simultaneously.
  - ✶ Java scripts runs when user clicks on/off push button at the *CAEN-SY4527-Expert Controls* CSS-BOY screen.
  - ✶ Not all HV boards’ channels responded to on/off commands.
    - ▪ This requires that commands are set several times to set all channels on/off.

- Developed *CAEN-SY4527-Expert Controls* CSS-BOY screen to control all HV boards' channels simultaneously.



- Tested 16 CAEN-A7030TN HV boards simultaneously under the following specifications:

Voltage Ramp Up/Down Test				
Mainframe Model	SY4527	**Set Voltage**		1500 V
Mainframe S/N	400	**Ramp Up/Down Rate**		25 V/s
Board Models	A7030TN	**Max Current Set**		1000 uA
Total Boards Tested	16	**Load: 0 Ω**	**Vmax: 1800 V**	**IMon**: ~ 0 uA
Total Channels Tested	576	**Total # Ramp Up/Down per channel**		1/1

  - ✶ Found that all HV boards have CAEN software issues with the exception of HV boards in slots #5, #9 and #14.
  - ✶ CAEN software issues consists mainly in the random changes of the parameters ("Vset", "Vmax","Iset", "VRUp", and "VRdwn") from its pre-set values.
- Generated spreadsheet with detailed results for all 16 HV boards
  - ✶ Spreadsheet contains the summary for test performed and screenshots of all Voltage Ramp Test CSS-BOY screens and GECO2020 parameters.
  - ✶ Screenshots for GECO2020 show initial set parameter before the test was started.

DSG R&D – cRIO Test Stands

- Began NI 9401 TTL Digital Input/Output module testing
  - ✶ Soldered D-sub connector to be used for module test setup.
  - ✶ Debugged FPGA programming issues caused by incorrect output assignment in the module settings.
- Testing of NI-9871 RS485 Serial module in progress.
  - ✶ Wired breakout board to connect the NI 9871 module to the USB-to-485 serial interface box.
  - ✶ Wrote LabVIEW program to write from the serial interface box to the module and from the module to the serial interface box.
  - ✶ Completed successfully test: read from module and write from module at 9600 Bd.

DSG R&D – LV Chassis FPGA

- Investigated MicroPython and add-on package for DE0-Nano-SOC board.
  - ✶ MicroPython is an implementation of Python specifically developed for microprocessors and SoCs
  - ✶ DE0-Nano-SOC add-on adds a library for communicating with board's FPGA from SoC.
  - ✶ Debugging issues with cross-compiler required to build MicroPython for board's SoC.
- Replicated LV cRIO's excitation program (program to set all sensor voltages/currents in Python).
  - ✶ Program runs on a desktop PC and communicates to LV Chassis via serial.
  - ✶ Program is first step in developing excitation program for SoC.
  - ✶ If MicroPython is usable on DE0-Nano-SOC, program will be reconfigured to read data directly from FPGA rather than through serial.
    - ▪ If MicroPython is not usable, program will be redeveloped in C since SoC has been proven to run C binaries.

Accelerator Division R&D

- Continued with the adjustments to the bonding parameters for superconducting Nb_3Sn strip resonator sample, no successful bonds yet.

DSG-RICH R&D

- Developed and debugged sbRIO FPGA code in LabVIEW to support the read-back and clearing of the temperature sensors' (Sensirion SHT85 sensors) status registers.

DSG R&D – PLC Test Station

- Setup communications between AB-L35E CompactLogic PLC and dgswin10 PC via RS232 serial protocol.
- Hooked up RTD temperature sensor.
- Wrote PLC program to read temperature values and average them together.